WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a memory cell array including a memory cell having a ferroelectric capacitor, the memory cell having a first electrode and a second electrode;

a first bit line electrically connected to the first electrode;

a second bit line complementary to the first bit line;

a first potential generation circuit which supplies a first potential to the second electrode to apply a voltage dropping at a first rate of change with a rise of temperature to the ferroelectric capacitor; and

a sense amplifier which amplifies a potential difference between the first bit line and the second bit line.

2. The device according to claim 1, wherein the first rate of change is equal to dependence on temperature possessed by a saturated voltage of the ferroelectric capacitor.

3. The device according to claim 1, further comprising:

a third potential generation circuit supplying a potential which rises at a third rate of change with the rise of temperature as a reference potential to the

second bit line.

4. The device according to claim 3, wherein the third rate of change is equal to a rate of change, which is dependant on the rise of temperature, of an intermediate value between a maximum value at a "0" data read time from the ferroelectric capacitor and a minimum value at a "1" data read time.

5. The device according to claim 1, wherein the first rate of change is imparted with a dependence on temperature so that an intermediate value between a maximum value when a "0" data is read from the ferroelectric capacitor and a minimum value when a "1" data is read is constant regardless of the temperature.

6. A semiconductor integrated circuit device comprising:

a memory cell array including a memory cell having a ferroelectric capacitor as a storage element, the memory cell having a first electrode and a second electrode;

a first bit line electrically connected to the first electrode;

a first bit line complementary to the first bit line;

a sense amplifier which amplifies a potential difference between the first bit line and the second bit line; and

a second potential generation circuit supplying a

voltage as a power potential of the sense amplifier, the voltage dropping at a second rate of change with a rise of temperature.

7. The device according to claim 6, wherein the second rate of change is equal to dependence on temperature possessed by a saturated voltage of the ferroelectric capacitor.

8. The device according to claim 6, further comprising:

a third potential generation circuit supplying a potential which rises at a third rate of change with the rise of temperature as a reference potential to the second bit line.

9. The device according to claim 8, wherein the third rate of change is equal to a rate of change, which is dependant on the rise of temperature, of an intermediate value between a maximum value at a "0" data read time from the ferroelectric capacitor and a minimum value at a "1" data read time.

10. The device according to claim 6, further comprising:

a first potential generation circuit which supplies a first potential to the second electrode to apply a voltage dropping at a first rate of change with the rise of temperature to the ferroelectric capacitor.

11. The device according to claim 10, wherein the second rate of change is equal to the first rate of

change.

12. The device according to claim 10, wherein the first rate of change or the second rate of change is equal to dependence on temperature possessed by a saturated voltage of the ferroelectric capacitor.

13. The device according to claim 10, further comprising:

a third potential generation circuit supplying a potential which rises at a third rate of change with the rise of temperature as a reference potential to the second bit line.

14. The device according to claim 13, wherein the third rate of change is equal to a rate of change, which is dependant on the rise of temperature, of an intermediate value between a maximum value at a "0" data read time from the ferroelectric capacitor and a minimum value at a "1" data read time.

15. The device according to claim 10, wherein the first rate of change is imparted with a dependence on temperature so that an intermediate value between a maximum value when a "0" data is read from the ferroelectric capacitor and a minimum value when a "1" data is read is constant regardless of the temperature.

16. A semiconductor integrated circuit device comprising:

a memory cell array including a memory cell having a ferroelectric capacitor as a storage element, the

memory cell having a first electrode and a second electrode;

a first bit line electrically connected to the first electrode;

a second bit line complementary to the first bit line; and

a circuit which supplies a first potential to the second electrode to read information, a time for which the first potential is supplied dropping with a rise of temperature.

17. The device according to claim 16, wherein a dependence on temperature of the time is equal to that of a time which the polarization of the ferroelectric capacitor needs to reverse.

18. A semiconductor integrated circuit device comprising:

a memory cell array including a memory cell having a ferroelectric capacitor as a storage element, the memory cell having a first electrode and a second electrode;

a first bit line electrically connected to the first electrode;

a second bit line complementary to the first bit line;

a first circuit which supplies a first potential to the second electrode to read information;

a sense amplifier which amplifies a potential

difference between the first bit line and the second
bit line; and

a second circuit which supplies a second potential
as a power potential of the sense amplifier, a time for
5  which the second potential is supplied dropping with a
rise of temperature after the first potential is set at
a low level.

19.  The device according to claim 18, wherein a
dependence on temperature of the time is equal to that
10  of a time which the polarization of the ferroelectric
capacitor needs to reverse.